REMARKS

Applicant respectfully requests reconsideration of this application. In the Office Action, claims 19-23, 93-105, and 107-118 were pending. No claim has been amended. Two new claims (claims 119, 120) have been added. No new matter has been added.

Rejections under 35 U.S.C. § 102

Claims 19, 20, 22, 93, 98, 99, 100, 101, and 109 are rejected under 35 U.S.C. §102(b) as being anticipated by Sidwell *et al.*, European Patent Application EP 0743594 A1, (herein referred to as Sidwell). Claim 19 recites:

> 19. A method comprising:
>
> **storing a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations in response to execution of a first instruction** that does not specify an order in which the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations; and
>
> duplicating bits from the plurality of non-contiguous groups of destination storage locations into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations.
>
> (emphasis added)

Applicant respectfully asserts that Sidwell fails to disclose at least "storing a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations in response to execution of a first instruction" and "duplicating bits from the plurality of non-contiguous groups of destination storage locations into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations" as required by claim 19.

The Office Action alleges claim 19 is anticipated by Sidwell with reference to Figure 6 and description about the "rep4p" instruction in Sidwell (Sidwell, page 6, lines 1-14). Applicant respectfully disagrees. The "rep4p" instruction describes storing S[0], S[1], S[2], and S[3] to R[0], R[1], R[2], and R[3] respectively as well as to R[4], R[5], R[6], and R[7] respectively (Sidwell, page 6, line 13). S[0], S[1], S[2], and S[3] are contagious groups of source bits. Therefore, Sidwell fails to disclose "storing a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations in response to execution of a first instruction".

The Office Action has failed to construe Sidwell correctly as described in Sidwell (page 5, line 45 – page 6, line 13) regarding the "byte replicate" instruction and its variants. None of the variants of the "byte replicate" instruction discloses operating on non-contiguous groups of source bits. A "rep2p" instruction, for example, operates on S[0] and S[1] which are contiguous to each other.

Additionally, claim 19, as recited, requires "duplicating bits from the plurality of non-contiguous groups of destination storage locations into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations". The Office Action alleges that the "rep4p" instruction of Sidwell discloses the limitation. Applicant respectfully disagrees. The "rep4p" instruction as explained above (Sidwell,

page 5, line 45 – page 6, line 13) is about storing S[0], S[1], S[2], and S[3] to R[0], R[1], R[2], and R[3] respectively as well as to R[4], R[5], R[6], and R[7] respectively. According to the example given by the Office Action, R[0] and R[3] are stored into locations R[4] and R[7] respectively. R[3] and R[4] are adjacent. However, the Office Action fails to recognize that R[7] (a destination storage location) is <u>not adjacent</u> to either [R0] or R[3]. Therefore, Sidwell fails to disclose "duplicating bits from the plurality of non-contiguous groups of destination storage locations into groups of destination storage locations <u>adjacent</u> to the non-contiguous groups of destination storage locations" as required by claim 19.

     In short, Sidwell discloses a "rep4p" instruction that moves contiguous source bits (S[0] to S[4]) to contiguous groups of destination storage location (R[0] to R[3]; R[4] to R[7]). Sidwell fails to disclose at least the two limitations as required in claim 19. For at least the foregoing reasons, Applicant believes that claim 19 is allowable. Applicant respectfully requests the withdrawal of the rejection for the claim 19. Moreover, dependent claims 20 and 22 depend from independent claim 19. Applicant believes that claim 19 is allowable such that claims 20 and 22 depending there from with additional limitations are also allowable.

     Similarly, independent claims 93 and 101 were rejected using the same example in the Office Action. The detailed remarks with respect to independent claim 19 are incorporated herein by reference. For the reasons similar to those discussed above, it is respectfully submitted that claims 93 and 101 are not anticipated by Sidwell. Claims 98, 99, 100, and 109 depend from one of the above independent claims. It is respectfully submitted that the claims are not anticipated by Sidwell. Accordingly, Applicant respectfully submits that claims 93, 98, 99, 100, 101, and 109 are patentable over the

cited reference, and respectfully requests the rejections of claims under 35 U.S.C. §102(b) be withdrawn.

Claims 110-118 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,115,812 of Abdallah *et al.* (hereinafter "Abdallah").

Claim 110, as presented, recites:

> 110. A machine-readable medium having stored thereon an instruction, which if executed by a machine, causes the machine to perform a method comprising:
>
> storing bits [31-0] of a source value into bit storage locations [63-32] and [31-0] of a destination register;
>
> storing bits [95-64] of the source value into bit storage locations [127-96] and [95-64] of the destination register, **wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register**. (emphasis added)

Applicant respectfully asserts that Abdallah fails to disclose at least "wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register" as required by claim 110. As explained in the Office Action, Abdallah only mentions that the operand source bits are copied to any location of the result. The Office Action agrees that Abdallah is silent about whether "an order must be directly specified in the instruction". Therefore, Abdallah fails to disclose at least "wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register" as required in claim 110. Applicant

would like to assert that a claim is anticipated only if each and every element as set forth
in the claim is found, either expressly or inherently described, in a single prior art
reference.

Furthermore, the Office Action has relied on an example therein that assumes
result 354 is "BBDD". However, referring to Abdallah (col. 6, line 44-55), the instruction
SHUFPS, as disclosed, moves source data having data items A, B, C, and D into a
destination register, with possibilities to occupy any location of a result data item (col.6,
line 49-50). Result 354 is unknown unless at least one operand (provided by the
programmer) is used to designate the order of data items (A, B, C, and D) when stored in
the destination register. When writing program, programmers provide sufficient operands
in a computer instruction for a computer to operate on. Applicant respectfully requests the
Office Action to explain why result 354 is to "BBDD" but not otherwise, such as other
possibilities listed in Abdallah (col. 6, line 55).

For at least the foregoing reasons, Applicant believes that claim 110 is allowable.
Applicant respectfully requests the withdrawal of the rejection for the claim 110.
Moreover, dependent claims 111 and 112 depend from independent claim 110. Applicant
believes that claim 110 is allowable such that claims 111 and 112 depending there from
with additional limitations are also allowable. Applicant respectfully requests the
rejections of claims 110-112 under 35 U.S.C. §102(b) be withdrawn.

Similarly, independent claims 113 and 116 were rejected using a similar example
in the Office Action. The detailed remarks with respect to independent claim 110 are
incorporated here by reference. For the reasons similar to those discussed above, it is
respectfully submitted that claims 113 and 116 are not anticipated by Abdallah. Claims
114 and 115 depend from independent claims 113. Claims 117 and 118 depend from

independent claim 116. Hence, it is respectfully submitted that the claims (114, 115, 117, and 118) are not anticipated by Abdallah. Accordingly, Applicant respectfully submits that claims 113-118 are patentable over the cited reference, and respectfully requests the rejections of the claims under 35 U.S.C. §102(b) be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 21, 23, 94-97, 102-105, 107 and 108 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sidwell *et al.*, European Patent Application EP 0743594 A1, (herein after Sidwell).

Claims 21, 23, 94-97, 102-105, 107, and 108 depending indirectly on independent claim 19, 93, or 101, are rejected under 35 U.S.C. 103(a) as being unpatentable over Sidwell. As presented above in traversing the 35 U.S.C rejections of the independent claim 19, Sidwell does not teach or suggest each and every limitation of independent claims 19, 93, and 101. No other reference was cited by the Examiner to cure those deficiencies of Sidwell. Thus, claims 21, 23, 94-97, 102-105, 107, and 108, which depend from the above independent claims, are patentable over Sidwell. Accordingly, Applicant respectfully request that the 35 U.S.C. §103(a) rejection of claims be withdrawn.

New Claims

Applicants present two new independent claims (119-120). The following remarks point out reasons these claims are believed to be allowable over the cited reference.

Claim 119, as presented, recites:

119. A machine-readable medium having stored thereon an instruction, which if executed by a machine, causes the machine to perform a method comprising:

storing bits [31-0] of a source value into bit storage locations [31-0] of a destination register;

duplicating bits from the bit storage locations [31-0] to bit storage locations [63-32] of the destination register;

storing bits [95-64] of the source value into bit storage locations [95-64] of the destination register; and

duplicating bits from the bit storage locations [95-64] to bit storage locations [127-96] of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register.

Sidwell describes the "rep4p" instruction that stores S[0], S[1], S[2], and S[3] to R[0], R[1], R[2], and R[3] respectively as well as to R[4], R[5], R[6], and R[7] respectively (Sidwell, page 6, line 13). Sidwell fails to disclose all limitations as required in claim 119.

Abdallah merely moves source data into the bit storage locations of a destination register. Abdallah does not duplicate the data from the bit storage locations of the destination register to adjacent bit storage locations. Hence, Abdallah fails to disclose "duplicating bits from the bit storage locations [31-0] to bit storage locations [63-32] of the destination register" and "duplicating bits from the bit storage locations [95-64] to bit storage locations [127-96] of the destination register".

Additionally, Abdallah fails to disclose at least "wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register" as required by claim 119. The detailed remarks with respect to independent claim 110 are incorporated herein by reference.

Claim 120, as presented, recites:

> 120. A machine-readable medium having stored thereon an instruction, which if executed by a machine causes the machine to perform a method comprising:
>
> storing bits [63-32] of a source value into bit storage locations [63-32] of a destination register;
>
> duplicating bits from the bit storage locations [63-32] to bit storage locations [31-0] of the destination register;
>
> storing bits [127-96] of the source value into bit storage locations [127-96] of the destination register; and
>
> duplicating bits from the bit storage locations [127-96] to bit storage locations [95-64] of the destination register, wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register.

Sidwell describes the "rep4p" instruction that stores S[0], S[1], S[2], and S[3] to R[0], R[1], R[2], and R[3] respectively as well as to R[4], R[5], R[6], and R[7] respectively (Sidwell, page 6, line 13). Sidwell fails to disclose all limitations as required in claim 120.

Abdallah merely moves source data into the bit storage locations of a destination register. Abdallah does not duplicate the data from the bit storage locations of the destination register to adjacent bit storage locations. Hence, Abdallah fails to disclose "duplicating bits from the bit storage locations [63-32] to bit storage locations [31-0] of the destination register" and "duplicating bits from the bit storage locations [127-96] to bit storage locations [95-64] of the destination register".

Additionally, Abdallah fails to disclose at least "wherein the instruction does not include a code to designate the order in which the source bits are to be stored in the destination register" as required by claim 120. The detailed remarks with respect to independent claim 110 are incorporated herein by reference.

For at least the foregoing reasons, Applicants believe claims 119-120 are allowable over the cited references, and respectfully request that the Examiner allow these claims.
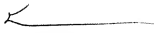
CONCLUSION

Applicant respectfully submits that the rejections have been overcome by the remarks, and that the pending claims are in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the pending claims be allowed.

Pursuant to 37 C.F.R. §1.136(a)(3), Applicants hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: _Oct 23_, 2008

Michael J. Mallie
Attorney for Applicant
Reg. No. 36,591

1279 Oakmead Parkway
Sunnyvale, California 94085-4040
(408) 720-8300